X-Wall LX SPECIFICATION

-- for system implementation with external key token as authentication

Customer's Name: _____

Product SKU (Stock Keeping Unit):
X-Wall LX-40 (Ultra DMA 66/100/133, DES 40-bit key strength)
X-Wall LX-64 (Ultra DMA 66/100/133, DES 64-bit key strength)
X-Wall LX-128 (Ultra DMA 66/100/133, TDES 128-bit key strength)
X-Wall LX-192 (Ultra DMA 66/100/133, TDES 192-bit key strength)

Product Description: Real-time IDE hard drive crypto bridge

Date of Approval: _____

Approved By: _____

Revision History

Rev No.	Description	Rev. Date
A	Initial release	07/01/03
A1	2nd Release with Secure Key token	07/02/03
A2	3rd Release with Secure Key token	07/09/03
A3	4th Release with Secure Key token	11/23/03

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1. Introduction

The ***X-Wall LX*** ASIC (Application Specific Integrated Circuit) family is engineered specifically to encrypt/decrypt the entire hard disk including boot sector and operating system with **real-time** performance using *NIST (The National Institute of Standards and Technology)* of the United States of America and *CSE (The Communications Security Establishment)* of the Government of Canada certified *DES* (Data Encryption Standard, http://csrc.nist.gov/cryptval/des/desval.html) and TDES (Triple DES, http://csrc.nist.gov/cryptval/des/tripledesval.html) algorithms.

X-Wall LX sits between the Host IDE and the Device IDE interface as a real-time IDE crypto gateway. It intercepts, interprets, translates, and relays those commands & data to and from the disk drives, encrypting the data with DES/TDES 40/64/128/192-bit key strengths. *X-Wall LX* can be operated with PIO, Ultra ATA (Ultra DMA) 66/100/133 compliant disk drives in ***real-time*** mode with an unprecedented throughput of 1.6 Gigabit/sec. The performance-optimized DES/TDES hardware engine performs all encryption and decryption operations. There is absolutely no software component, which entirely eliminates all memory and interrupt overheads.

X-Wall LX requires no device drivers and is independent from, and invisible to, all operating systems. As long as the drive is Ultra ATA 66/100/133 compliant, *X-Wall LX* will work in the system. Once authenticated, its operation is completely transparent to all users and does not require any form of management or intervention, as is normal with complex Graphical User Interfaces (GUIs) as found in other solutions.

X-Wall LX is supplied with a pair of portable ***X-Wall Secure Keys*** which load device status and, most importantly, the DES/TDES "Secret Key." The *X-Wall Secure KEY* serves as an exclusive device for authentication from which the *X-Wall Secure Key* must present itself to activate *X-Wall LX*.

This design guide recommends system-based design issues with *X-Wall LX*. It further provides guidelines for IDE connector cabling, component and resistor placement, signal termination and trace routing for both IDE interfaces (from Host and to Device). The following table shows the currently available *X-Wall SE* and *X-Wall LX* family microchips. Please note, all *X-Wall SE* series chips are pin-to-pin compatible. Likewise, all *X-Wall LX* series chips are pin-to-pin compatible. However, the pin assignment of LX is different from that of SE. The major differences between the *X-Wall LX* and *X-Wall SE* are listed below.

	Cipher Engine Transfer Rate	Ultra ATA Protocols Supported	Required External OSC?	Core Voltage	Secure Key Voltage
X-Wall LX	**1.6 Gigabit/sec**	**ATA 6, Mode 6 transfer Compatible**	**NO, just crystal**	**+3.3V**	**+3.3V/5V**

		with all ATA 66/100/133			
X-Wall SE	**1.1 Gigabit/sec**	**ATA 5, Mode 4 transfer Compatible with all Ultra ATA 33/66/100**	**YES, 66MHz OSC required**	**+5V**	**+5V**

Table 1. The major differences between the *X-Wall LX and SE*

X-Wall	**Key Strength**	**NIST[1] & CSE[2] Certified 100% hardware Cipher Engine**	**Maximum Throughput**	**Ultra ATA hard disk support**	**Ultra ATA hard disk compliance**	**Protocol & Transfer mode support up to**	**Package**
SE-40NB	40-bit	**DES**	712 Mbit/sec	< 137GB	33, 66	ATA 5, Mode 4 transfer	128-pin LQFP
SE-64NB	64-bit	**DES**	712 Mbit/sec	< 137GB	33, 66	ATA 5, Mode 4 transfer	128-pin LQFP
SE-40A	40-bit	**DES**	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP
SE-64A	64-bit	**DES**	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP
SE-128A	128-bit	**TDES**	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP
SE-192A	192-bit	**TDES**	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP
LX-40	40-bit	**DES**	1.6 Gbit/sec	> 137GB	66, 100, 133	ATA 6, Mode 6 transfer	128-pin LQFP
LX-64	64-bit	**DES**	1.6 Gbit/sec	> 137GB	66, 100, 133	ATA 6, Mode 6 transfer	128-pin LQFP
LX-128	128-bit	**TDES**	1.6 Gbit/sec	> 137GB	66, 100, 133	ATA 6, Mode 6 transfer	128-pin LQFP
LX-192	192-bit	**TDES**	1.6 Gbit/sec	> 137GB	66, 100, 133	ATA 6, Mode 6 transfer	128-pin LQFP

Table 2. The X-Wall SE and X-Wall LX Family Microchips

System Requirement

- All operating systems
- Ultra ATA (Ultra DMA) 66/100/133 compliant hard disk drive
- Motherboard with standard IDE interface
- One disk drive per *X-Wall LX*
- Does NOT support ATAPI devices such as CD-ROM, CD-R, CD-RW, DVD-ROM or DVD-RW

[1] NIST – The National Institute of Standards and Technology of the United States of America
[2] CSE – The Communications Security Establishment of the Government of Canada

2. System Configurations

2.1 Disk Drive Configurations

The configuration of the *X-Wall LX* controlled hard disk drive is flexible. You may choose one of the four configurations shown in **Table 3. Selectable disk drive configuration.** This may be done by using hardware jumpers found on the disk drive.

X-Wall LX	Primary	Secondary
Master	Yes, as a secure boot drive	Yes, as a secure data drive
Slave	Yes, as a secure data drive	Yes, as a secure data drive

Table 3. Selectable disk drive configuration

2.2 System Configurations

There are two alternate connections of *X-Wall LX* with the Host IDE and the Device IDE. As shown in **Figure 1. One *X-Wall* & One IDE Device**, a typical configuration is comprised with only one IDE device in either one of the two IDE channels supported by the IDE host controller. The drive controlled by *X-Wall LX* is fully encrypted. The alternative configuration shown in **Figure 2. One *X-Wall* & Two IDE Devices** shows two IDE devices and only one *X-Wall LX* in one of the two IDE channels supported by the IDE host controller. The drive controlled by *X-Wall LX* is fully encrypted. However, the drive that is placed in front of *X-Wall LX* stores only clear text and is therefore an unencrypted drive. Encrypted and non-encrypted text may be exchanged by simply dragging and dropping files.

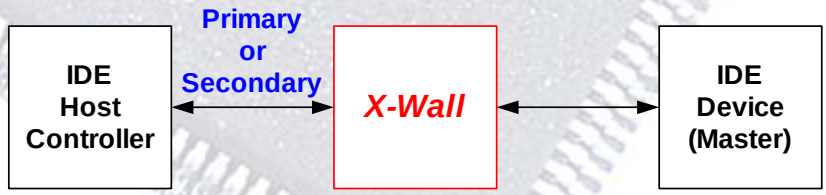


Figure 1. One X-Wall and One IDE Device

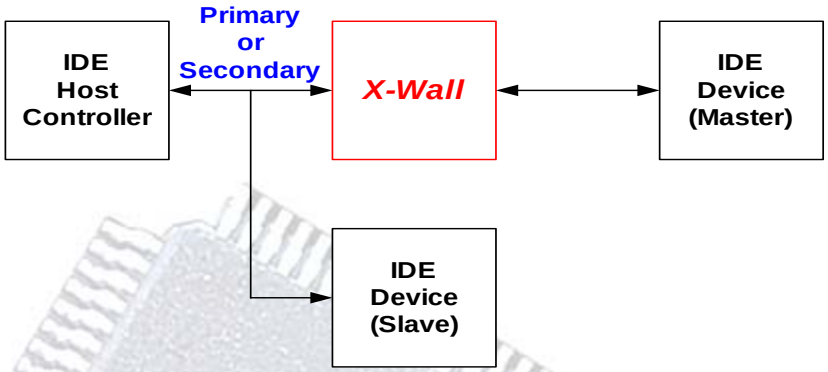


Figure 2. One X-Wall and Two IDE Devices

2.3 IDE Cables

The Ultra ATA 66/100/133 transfer modes require an 80-conductor cable (as shown in **Figure 3. A standard 80-conductor cable**) whereas Ultra ATA 33 and below (including PIO) require a 40-conductor cable instead (as shown in **Figure 4. A standard 40-conductor cable**).

An 80-conductor IDE cable uses the same 40-pin connector as the 40-conductor IDE cable. The wires of the 80-conductor cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard or circuit board through the ground pins in the 40-conductor Connector).

To determine whether Ultra DMA transfer modes greater than 2 (Ultra ATA/33, 33MB/sec transfer rate) may be enabled, the host requires the system software to attempt to determine the cable type used in the system through **Pin 34** of the connector as shown **in Figure 3. A standard 80-conductor cable**. If the system software detects an 80-conductor cable, the system may use any one of all the available Ultra DMA transfer modes up to the highest transfer mode supported by both the Southbridge chipset and the IDE device. If a 40-conductor cable is detected, the system software CANNOT enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

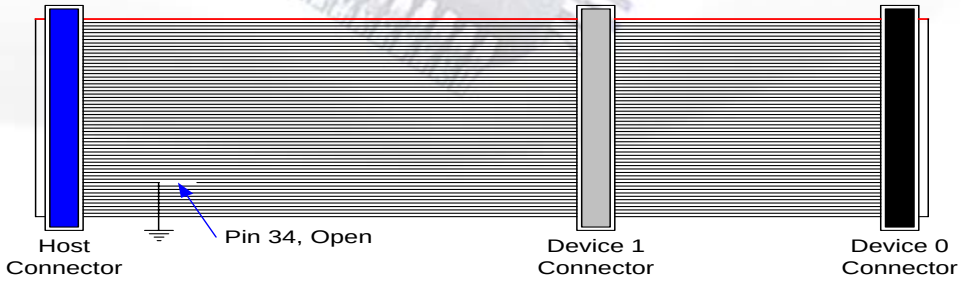


Figure 3. A standard 80-conductor cable (Pin 34 is grounded inside the 40-pin connector)

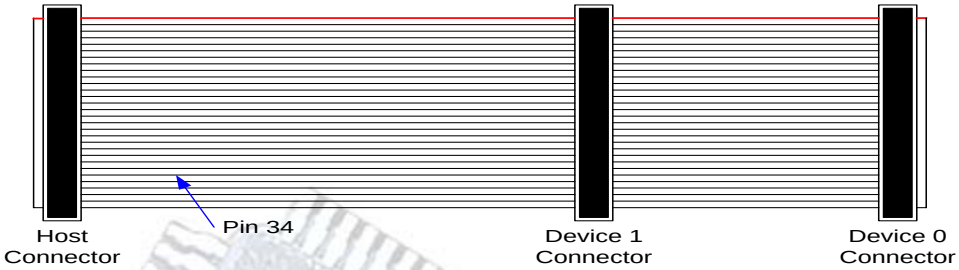


Figure 4. A standard 40-conductor cable (Pin 34 is NOT grounded)

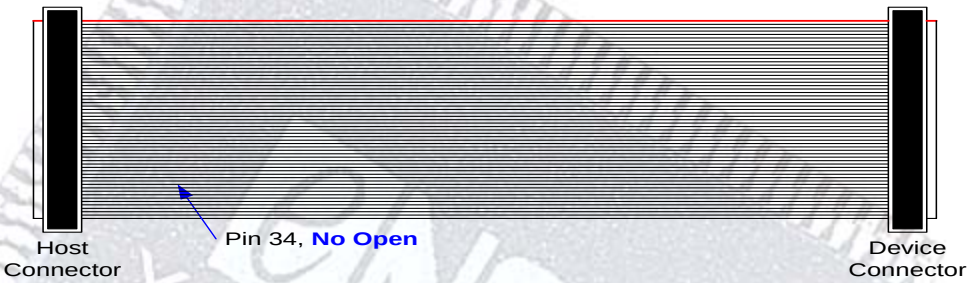


Figure 5. Enova specifically assembled 80-conductor cable (Pin 34 is NOT grounded)

If the system configuration is composed of one *X-Wall LX* and two IDE devices as shown in **Figure 2. One X-Wall and Two IDE Devices**, it is recommended that the system maker should provide one Enova specifically-assembled 80-conductor cable as shown **in Figure 5. Enova specifically assembled 80-conductor cable**. The suggested connection with two IDE devices on the same channel is shown in **Figure 6. Suggested cable connection** to avoid possible technical difficulties.

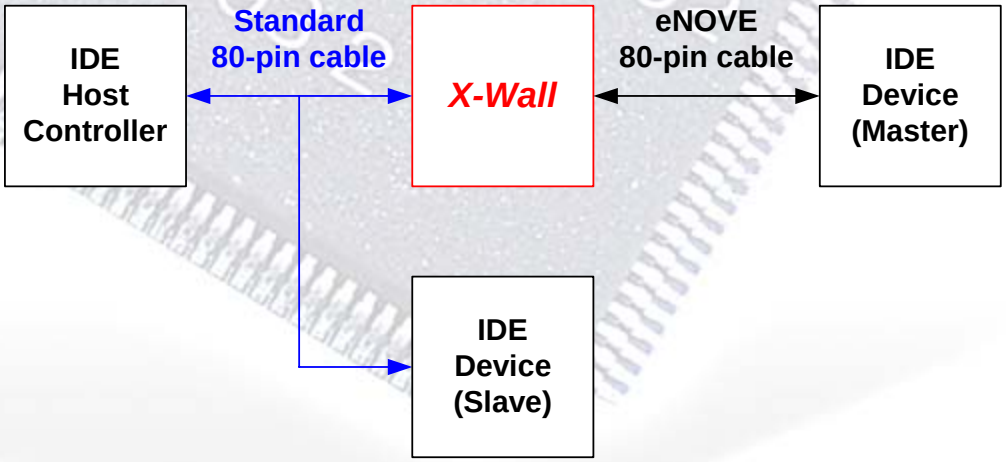
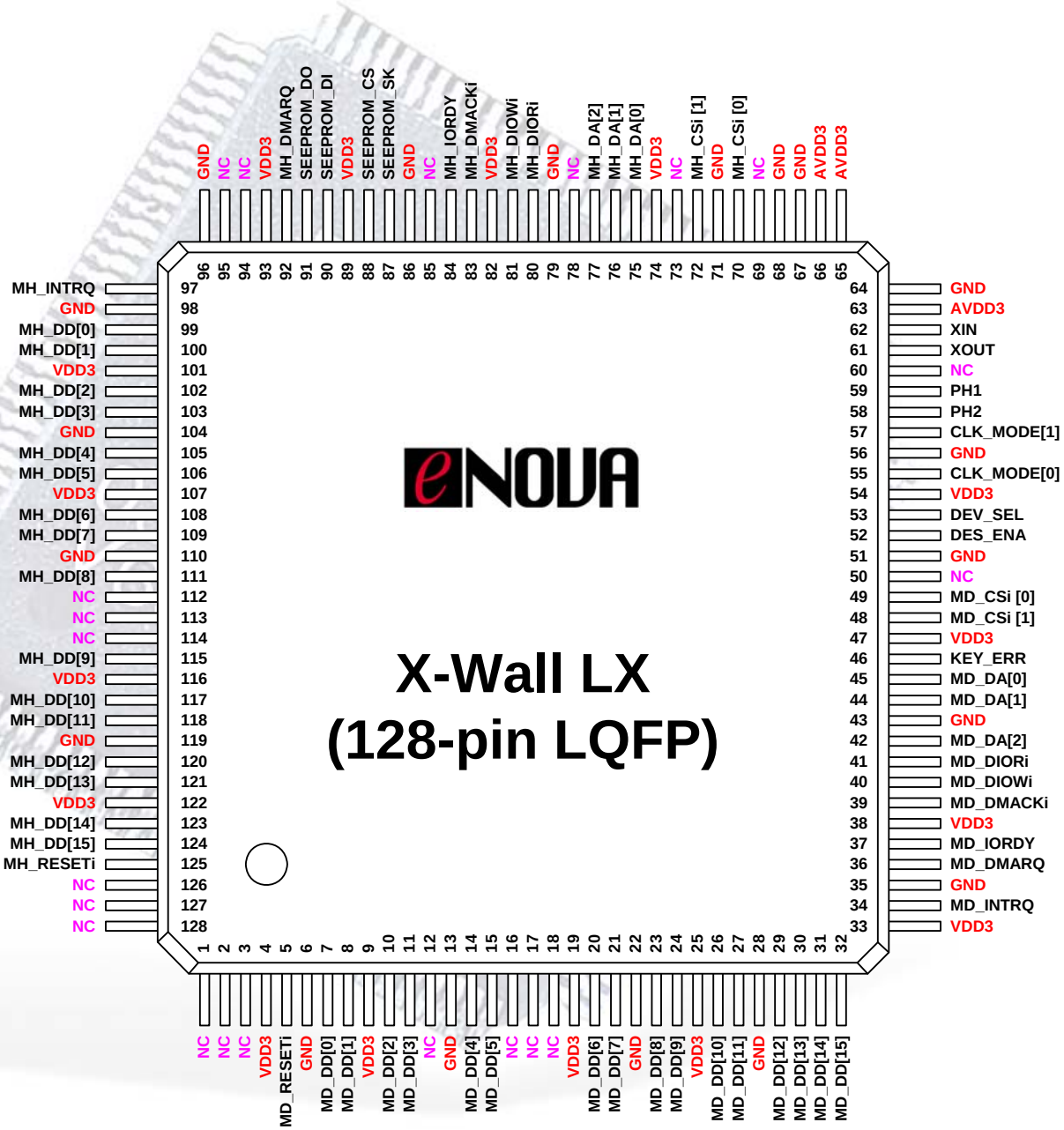


Figure 6. Suggested cable connection

3. X-Wall LX Pin Definition & Description

3.1 Pin Assignment

All X-Wall LX family microchips (including LX-40, LX-64, LX-128 and LX-192) share the same pin assignment and pin definition.



3.2 Pin Definition & Description

	Pin Names	I/O	Pin No.	Description
Host IDE	MH_CSi[1:0]	I	72,70	Chip select 1 & Chip select 0 driven by the host

Interface **(From South Bridge IDE Host Interface)**	MH_DD[15:0]	IO	124,123,121, 120,118,117, 115,111,109, 108,106,105, 103,102,100, 99	IDE Data Driven by the host and X-Wall
	MH_DA[2:0]	I	77-75	IDE address driven by the host
	MH_DMACKi	I	83	IDE DMA acknowledge driven by host
	MH_DMARQ	O	92	IDE DMA request driven by X-Wall
	MH_INTRQ	O	97	IDE Interrupt request driven by X-Wall
	MH_DIORi	I	80	Driven by host, internally split into: for PIO : MH_DIORi for uDMA data-in : MH_HDMARDYi for uDMA data-out : MH_HSTROBE
	MH_IORDY	O	84	Driven by X-Wall, one of the 3 signals is selected: for PIO : MH_IORDY for uDMA Data-In : MH_DSTROBE for uDMA Data-Out : MH_DDMARDYi
	MH_DIOWi	I	81	Driven by host, internally split into: for PIO : MH_DIOWi for uDMA, Data-In, Data-Out : MH_STOP
	MH_RESETi	I	125	Host reset signal
Device IDE Interface **(To Hard Disk Drive)**	MD_CSi[1:0]	O	48, 49	Chip select 0 & Chip select 1 driven by the X-Wall
	MD_DD[15:0]	IO	32-29,27,26, 24,23,21,20, 15,14,11,10, 8,7	IDE Data Driven by both X-Wall and Device
	MD_DA[2:0]	O	42, 44, 45	IDE address driven by X-Wall
	MD_DMACKi	O	39	IDE DMA acknowledge driven by X-Wall
	MD_DMARQ	I	36	IDE DMA request driven by Device
	MD_INTRQ	I	34	IDE Interrupt request driven by Device
	MD_DIORi	O	41	Driven by X-Wall, one of the 3 signals is selected: for PIO : MD_DIORi for uDMA data-in : MD_HDMARDYi for uDMA data-out : MD_HSTROBE
	MD_IORDY	I	37	Driven by X-Wall, internal split into: for PIO : MD_IORDY for uDMA Data-In : MD_DSTROBE for uDMA Data-Out : MD_DDMARDYi
	MD_DIOWi	O	40	Driven by X-Wall, one of the 2 signals is selected: for PIO : MD_DIOWi for uDMA, Data-In, Data-Out : MD_STOP
	MD_RESETi	O	5	Driven by X-Wall, reset signal

Power Pins	VDD3	P	4,9,19,25,33, 38,47,54,74, 82,89,93,101, 107,116,122	Power Supply (+3.3V) (Digital)
	AVDD3	P	63,65,66	Power Supply (+3.3V) (Analog)
	GND	P	6,13, 22, 28, 35, 43, 51, 56, 64, 67, 68, 71, 79, 86, 96, 98, 104, 110, 119	Ground
X-Wall Secure Key Interface	SEEPROM_SK	O	87	Key serial data clock
	SEEPROM_CS	O	88	Key chip select
	SEEPROM_DI	O	90	Key serial data input
	SEEPROM_DO	I	91	Key serial data output
	Note: X-Wall Secure Key Interface requires either +3.3V or +5V power supply, depending on the SEEPROM type you've chosen.			
Others	CLK_Mode[1:0]	I	57, 55	00:Reserved; 01:66MHz; 10:100MHz; 11:133MHz.
	PH1 PH2	I	58 59	PULL-HIGH (10KΩ)
	DES_ENA	I	52	PULL-HIGH for encrypt/decrypt operation
	KEY_ERR	O	46	Output high for key not existed or key parity error
	DEV_SEL	I	53	Device select; high for master, low for slave.
	XIN	I	62	Crystal input pad (14.318MHz)
	XOUT	O	61	Crystal output pad
	NC		1-3, 12, 16-18, 50, 60, 69,73, 78, 85, 94, 95,112-114, 126-128	No connection

3.3 Electrical Characteristics

- Operating Voltage (Vcc): +3.0V ~ +3.6V
- Temperature limit rating:
  - Storage temperature: -55°C ~ +125 °C
  - Operating temperature: 0°C ~ +70 °C
- PIO mode uses 40-conductor cable
- UDMA mode 0, 1, 2, 3, 4, 5 and 6 uses 80-conductor cable

4. Layout & Package Information

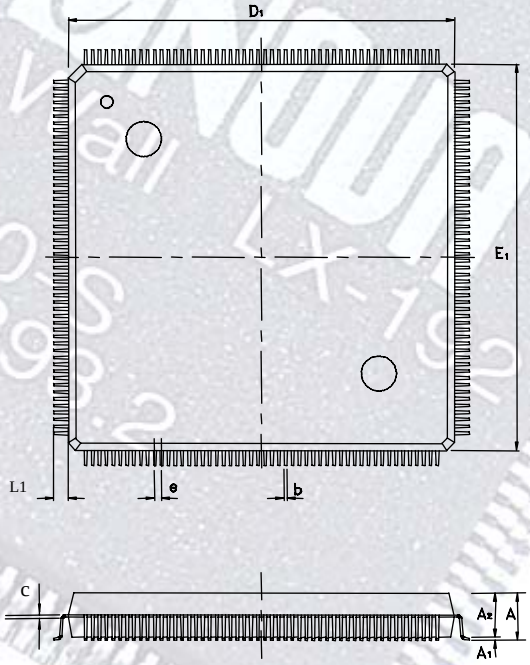
4.1 128-pin LQFP

LQFP (Low Profile Quad Flat Package) provides low profile 1.4mm body thickness, suitable for limited space environments. Package size 14×14mm and lead-count 128 are offered for portable, lightweight and low profile applications.

4.2 FEATURES

- 14×14mm body size with 128 lead count
- Copper leadframe
- Low profile 1.40mm body thickness
- JEDEC standard outlines

4.3 Outline & Dimension



Body Size	Lead Count	L/F Material	Lead Pitch	PKG Thk.	Stand Off	Body Thk.	Lead Length	Lead Width	L/F Thk.
D1 E1	N		e	A(Max.)	A1(Min.)	A2	L1	B	C
14 14	128	Cu:C7025	0.40	1.60	0.05	1.40	1.00	0.18	0.127

5. Platform Placement

Signal arrangement of the *X-Wall LX* is shown in **Figure 7. Signal arrangement of *X-Wall LX***.

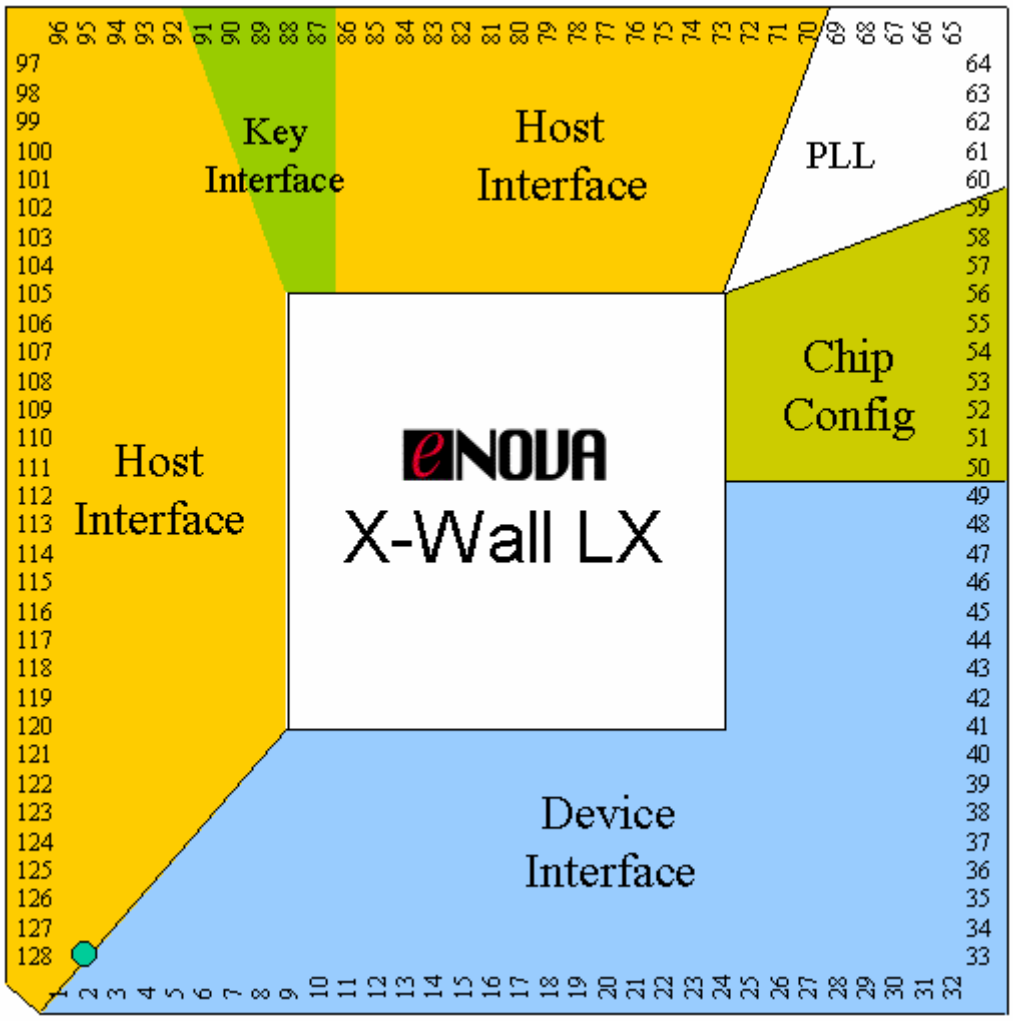


Figure 7. Signal arrangement of *X-Wall LX*

6. Reliability Tests

6.1 Product Life Test

Test Items	Test Condition/Result	Reference Standard
Operating Life	TA=125℃ ,1000Hours PASS	JESD22-A108-A

6.2 Electrical Test

Test Items	Test Condition/Result	Reference Standard
ESD	Level II	MIL-STD-883E 3015.7 JEDEC EIA/JESD22-A115
Latch-up	Level II	JEDEC-STD NO 78

6.3 Packaging Test

Test Items	Test Condition	Reference Standard
Thermal Shock	-65 Deg C/+150 Deg C 5min within 10 sec 5min 300 Cycles	MIL-STD-883E 1011.9
Temp. Cycling	-65 Deg C/+150 Deg C 1000 Cycles	MIL-STD-883E 1010.7
Pressure Cooker	121 Deg C,15 psig (2atm) 100% R.H. 216 hours	JEDEC-STD A102-2
Salt Atmosphere	35 Deg C,0.5%~3% NaC1 PH6.5~7.2 24 hours	MIL-STD-883E 1009.8
HAST	T_A=130 Deg C,85%R.H. 64 hours	JEDEC-STD NO. 22-A110

7. Marking Description

X-Wall LX-40

LX – version
40 – DES 40-bit strength

X-Wall LX-64

LX – version
64 – DES 64-bit strength

X-Wall LX-128

LX – version
128 – TDES 128-bit strength

X-Wall LX-192

LX – version
192 – TDES 192-bit strength

0320-S

0320 -- Year and Week of manufacturing date; Year 2003 on Week 20th
S -- Package & assembly House; SPIL

V60893.2 – Silicon Wafer Lot Number

8. Logistics

Package	Dimension	Capacity (Max.)
Tray	14*14*1.4 mm,6*15 grid, black	90ea
Inner Box	360*152*87 mm, white	900ea
Carton	375*333*290 mm, white	5400ea

9. Standard Material

Chip	Non-epi wafer + TSMC process
Lead frame	Copper
Die Attach Adhesive	Silver paste
Bonding Wire	Gold
Encapsulant	Mold Compound
Lead Finish	85/15 Sn/Pb