



## **X-Wall SE SPECIFICATION**

-- for system implementation with external key token as authentication

Customer's Name: \_\_\_\_\_

Product SKU (Stock Keeping Unit):

*X-Wall SE-40NB (Ultra DMA 33/66, DES 40-bit key strength)*

*X-Wall SE-64NB (Ultra DMA 33/66, DES 64-bit key strength)*

*X-Wall SE-40A (Ultra DMA 33/66/100, DES 40-bit key strength)*

*X-Wall SE-64A (Ultra DMA 33/66/100, DES 64-bit key strength)*

*X-Wall SE-128A (Ultra DMA 33/66/100, TDES 128-bit strength)*

*X-Wall SE-192A (Ultra DMA 33/66/100, TDES 192-bit key strength)*

Product Description: Real-time IDE hard drive crypto bridge

Date of Approval: \_\_\_\_\_

Approved By: \_\_\_\_\_

### **Revision History**

Rev No.	Description	Rev. Date
0.1	Initial release	2002/06/01
0.2	2 <sup>nd</sup> release	2002/08/15
0.3	3 <sup>rd</sup> release	2002/10/02
0.4	4 <sup>th</sup> release	2002/11/15
0.5	5 <sup>th</sup> release	2003/03/10
0.6	6 <sup>th</sup> release	11/23/2003



#### **Asia Operation**

Enova Technology Corporation  
Bldg. 53, #195-57, Sec. 4, Chung Hsing Rd., Chutung  
Hsin-Chu county, Taiwan 310, ROC  
Tel. +886 3 591 0197  
Fax +886 3 591 0204  
<http://www.enovatech.net>  
[info@enovatech.net](mailto:info@enovatech.net)

#### **North America Operations**

Enovatech, Inc. (Enova Technology)  
1072 Yosemite Drive  
Milpitas, California 95035, USA  
Tel. +1 408.956.8100  
Fax +1 408.956.8102  
<http://www.enovatech.com>  
[info@enovatech.com](mailto:info@enovatech.com)

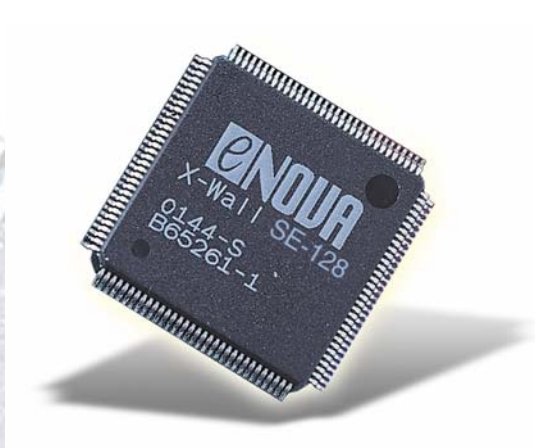


## Table of Content

<b>1. Introduction</b> .....	3
<b>2. System Configurations</b> .....	5
<b>2.1 Disk Drive Configurations</b> .....	5
<b>2.2 System Configurations</b> .....	5
<b>2.3 IDE Cables</b> .....	6
<b>3. X-Wall SE Pin Definition &amp; Description</b> .....	8
<b>3.1 Pin Assignment</b> .....	8
<b>3.2 Pin Definition &amp; Description</b> .....	8
<b>3.3 Electrical Characteristics</b> .....	10
<b>4. Layout &amp; Package Information</b> .....	11
<b>4.1 128-pin LQFP</b> .....	11
<b>4.2 FEATURES</b> .....	11
<b>4.3 Outline &amp; Dimension</b> .....	11
<b>5. Platform Placement</b> .....	12
<b>6. Reliability Tests</b> .....	13
<b>6.1 Product Life Test</b> .....	13
<b>6.2 Electrical Test</b> .....	13
<b>6.3 Packaging Test</b> .....	13
<b>7. Marking Description</b> .....	14
<b>8. Logistics</b> .....	14
<b>9. Standard Material</b> .....	15
<b>10. Secure Key Specification</b> .....	15



## 1. Introduction



The **X-Wall SE** ASIC (Application Specific Integrated Circuit) family is engineered specifically to encrypt/decrypt the entire hard disk bit by bit including boot sector and operating system with **real-time** performance using **NIST (National Institute of Standards and Technology)** certified **DES** (Data Encryption Standard, <http://csrc.nist.gov/cryptval/des/desval.html>) and **TDES** (Triple DES, <http://csrc.nist.gov/cryptval/des/tripledesval.html>) algorithms.

The **X-Wall SE** sits between Host IDE and the Device IDE interface as the real-time IDE crypto gateway. It intercepts, interprets, translates, and relays those commands & data to and from the disk drives, encrypting the data with DES/TDES 40/64/128/192-bit key strength. The **X-Wall SE** can be operated with PIO, Ultra ATA (Ultra DMA) 33/66/100 and native mode IDE compliant disk drives in **real-time** mode with an unprecedented throughput of 1.1 Giga bit per second. The performance-optimized DES/TDES hardware core performs all encryption and decryption. There is absolutely no software component, eliminating entirely the memory and interrupt overheads.

X-Wall requires no device driver and is independent from and invisible to all operating systems. As long as the drive is Ultra ATA 33/66/100 compliant, **X-Wall SE** will work in the system. Once authenticated, its operation is completely transparent to all users who do not require managing usually seen complex Graphical User's Interface (GUI) of other solutions.

X-Wall comes with a pair of portable **Enova Secure Key** that loads device status and most importantly, the DES/TDES "Secret Key." The **Enova Secure KEY** serves as an exclusive device for authentication from which the **Enova Secure Key** must present itself to activate the **X-Wall SE**.

This design guide recommends system based design issues with the **X-Wall SE**. It further provides guidelines for IDE connector cabling, component and resistor placement, signal termination and trace routing for both IDE interfaces (from Host and to Device). The following table shows the current available X-Wall SE family microchips.

<b>X-Wall</b>	<b>Key Strength</b>	<b>NIST<sup>1</sup> &amp; CSE<sup>2</sup> Certified 100% hardware Cipher Engine</b>	<b>Maximum Throughput</b>	<b>Ultra ATA hard disk support</b>	<b>Ultra ATA hard disk compliance</b>	<b>Protocol &amp; Transfer mode support up to</b>	<b>Package</b>
<b>SE-40NB</b>	40-bit	<b>DES</b>	712 Mbit/sec	< 137GB	33, 66	ATA 5, Mode 4 transfer	128-pin LQFP
<b>SE-64NB</b>	64-bit	<b>DES</b>	712 Mbit/sec	< 137GB	33, 66	ATA 5, Mode 4 transfer	128-pin LQFP
<b>SE-40A</b>	40-bit	<b>DES</b>	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP
<b>SE-64A</b>	64-bit	<b>DES</b>	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP
<b>SE-128A</b>	128-bit	<b>TDES</b>	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP
<b>SE-192A</b>	192-bit	<b>TDES</b>	1.1 Gbit/sec	< 137GB	33, 66, 100, 133	ATA 5, Mode 4 transfer	128-pin LQFP

**Table 1. The X-Wall SE Family Microchips**

**System Requirement**

- ❑ All operating systems
- ❑ Ultra ATA (Ultra DMA) 33/66/100 compliant hard disk drive
- ❑ Motherboard with standard IDE interface
- ❑ One disk drive per X-Wall SE
- ❑ Does NOT support ATAPI devices such as CD-ROM, CD-R, CD-RW, DVD-ROM or DVD-RW

<sup>1</sup> NIST – The National Institute of Standards and Technology of the United States of America

<sup>2</sup> CSE – The Communications Security Establishment of the Government of Canada

## 2. System Configurations

### 2.1 Disk Drive Configurations

The configuration of the X-Wall SE controlled hard disk drive is flexible. You may choose one from the four configurations as shown in Table 2. **Selectable disk drive configuration.** This may be done by using hardware jumpers on the disk drive.

X-Wall SE	Primary	Secondary
Master	Yes, as a <b>secure boot drive</b>	Yes, as a secure data drive
Slave	Yes, as a secure data drive	Yes, as a secure data drive

Table 2. Selectable disk drive configuration

### 2.2 System Configurations

There are two alternate connections of X-Wall SE with the Host IDE and the Device IDE. As shown in Figure 1. **One X-Wall & One IDE Device**, a typical configuration is comprised with only one IDE device in one of the two IDE channels supported by the IDE host controller. The alternative as shown in Figure 2. **One X-Wall & Two IDE Devices** shows two IDE devices and only one X-Wall in one of the two IDE channels supported by the IDE host controller.

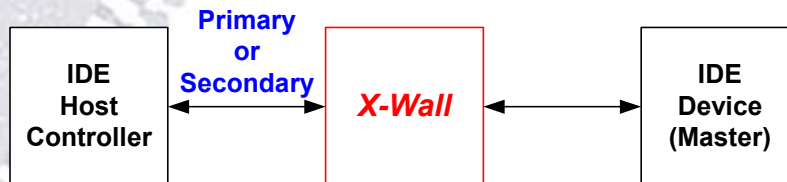


Figure 1. One X-Wall and One IDE Device

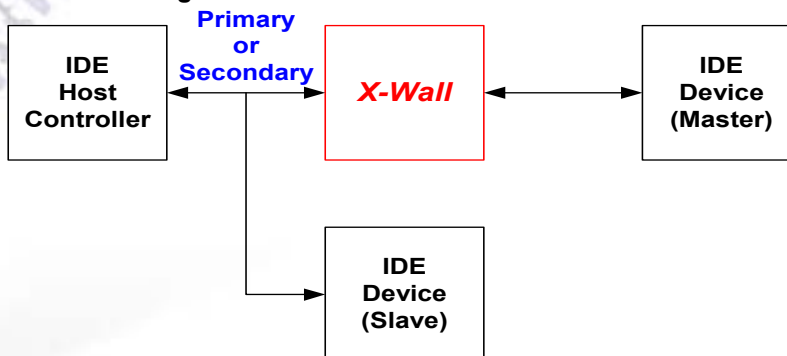


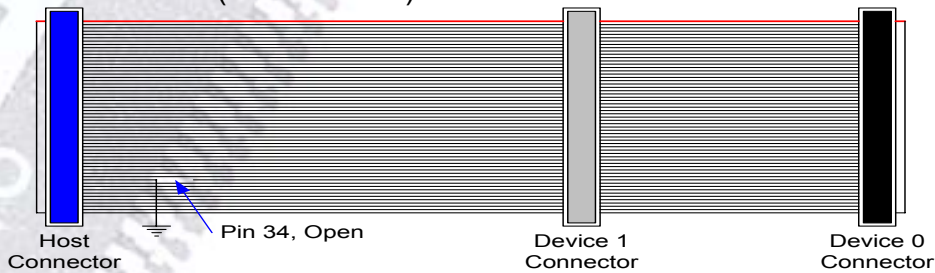
Figure 2. One X-Wall and Two IDE Devices

### 2.3 IDE Cables

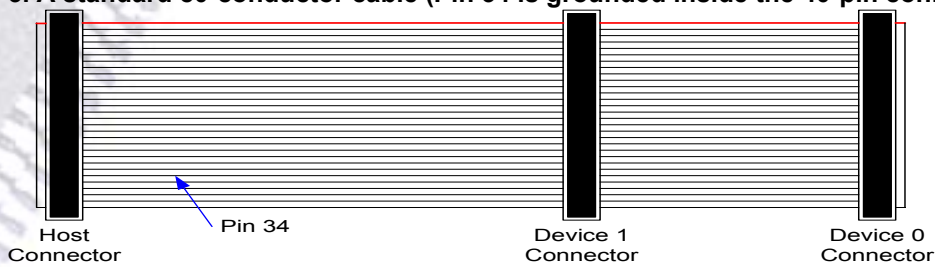
The Ultra ATA 66/100 transfer modes require an 80-conductor cable (as shown in **Figure 3. A standard 80-conductor cable**) whereas Ultra ATA 33 and below (including PIO) only demand a 40-conductor cable (as shown in **Figure 4. A standard 40-conductor cable**).

An 80-conductor IDE cable uses the same 40-pin connector as the 40-conductor IDE cable. The wires of the 80-conductor cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard or circuit board through the ground pins in the 40-conductor Connector).

To determine that if Ultra DMA transfer modes greater than 2 (Ultra ATA/33) can be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system through **Pin 34** of the connector as shown in **Figure 3. A standard 80-conductor cable**. If the system software detects an 80-conductor cable, the system may use any one of all the available Ultra DMA transfer modes up to the highest transfer mode supported by both the south bridge chipset and the IDE device. If a 40-conductor cable is detected, the system software can NOT enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).



**Figure 3. A standard 80-conductor cable (Pin 34 is grounded inside the 40-pin connector)**



**Figure 4. A standard 40-conductor cable (Pin 34 is NOT grounded)**

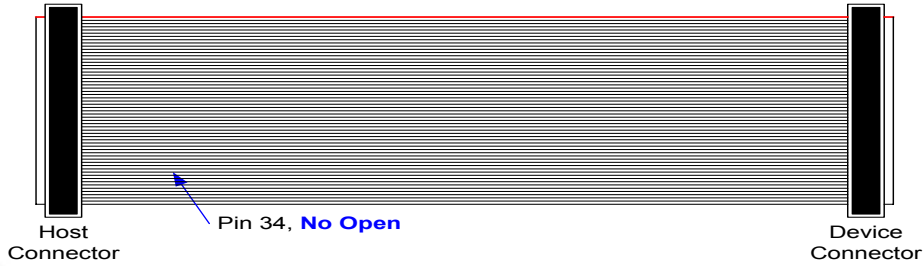


Figure 5. Enova specifically assembled 80-conductor cable (Pin 34 is NOT grounded)

If the system configuration is comprised with one *X-Wall SE* and two IDE devices as shown in Figure 2. **One X-Wall and Two IDE Devices**, we suggest that the system maker should provide one Enova specifically assembled 80-conductor cable as shown in Figure 5. Enova specifically assembled 80-conductor cable. The suggested connection with two IDE devices on the same channel is shown in Figure 6. Suggested cable connection to avoid possible technical problems.

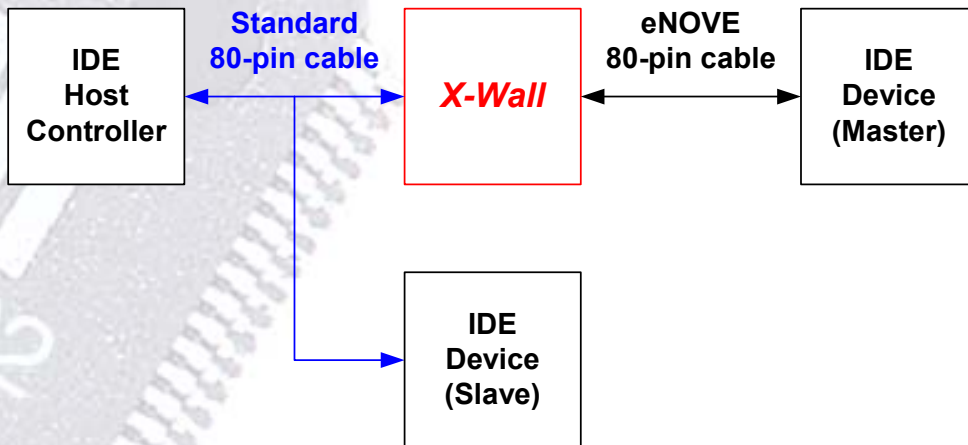
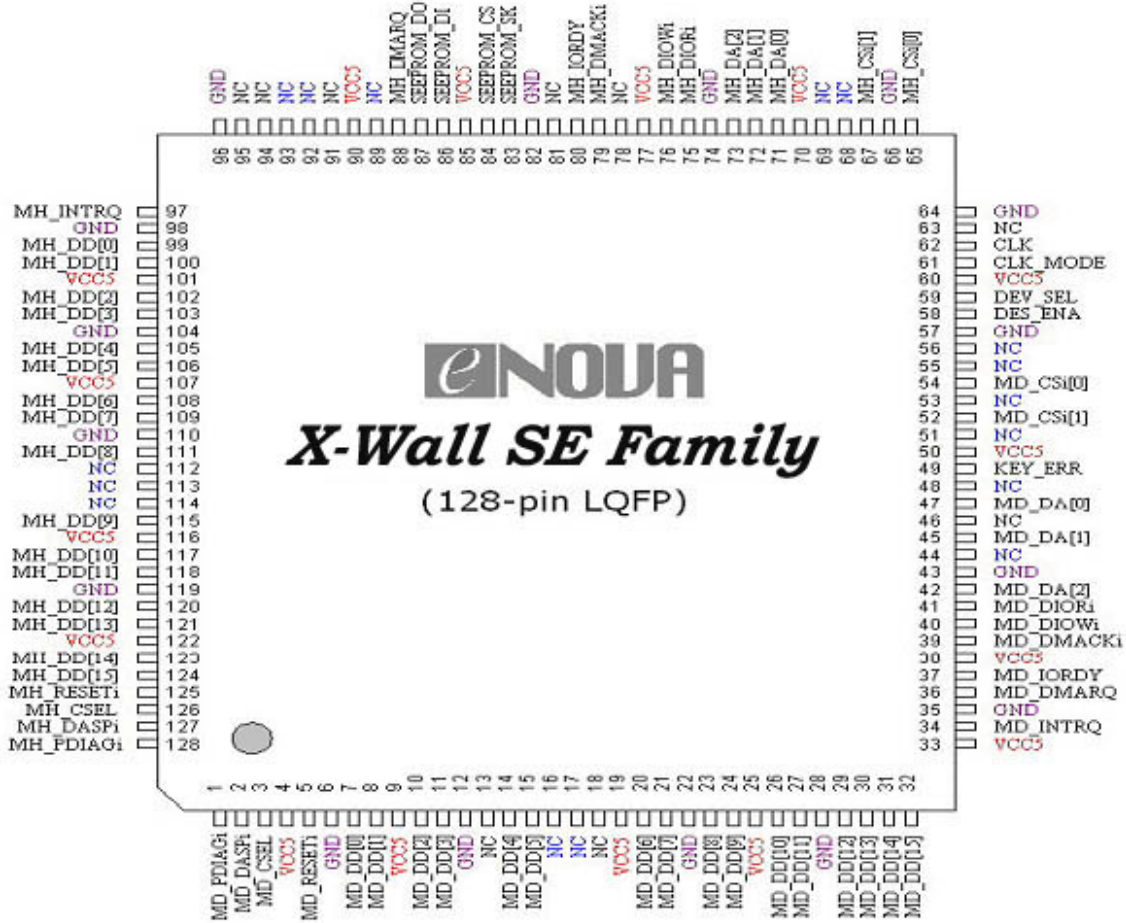


Figure 6. Suggested cable connection

### 3. X-Wall SE Pin Definition & Description

#### 3.1 Pin Assignment

All X-Wall SE family microchips (including SE-40NB, SE-64NB, SE-40A, SE-64A, SE-128A and SE-192A) share the same pin assignment and pin definition.



#### 3.2 Pin Definition & Description

	Pin Names	I/O	Pin No.	Description
Host IDE Interface  (From South Bridge IDE Host Interface)	MH_CSi[1:0]	I	67,65	Chip select 0 & Chip select 1 driven by the host
	MH_DD[15:0]	IO	124,123,121, 120,118,117, 115,111,109, 108,106,105, 103,102,100, 99	IDE Data Driven by the host and X-Wall
	MH_DA[2:0]	I	73-71	IDE address driven by the host
	MH_DMACKi	I	79	IDE DMA acknowledge driven by host



	MH_DMARQ	O	88	IDE DMA request driven by X-Wall
	MH_INTRQ	O	97	IDE Interrupt request driven by X-Wall
	MH_DIOR <sub>i</sub>	I	75	Drive by host, internally split into: for PIO : MH_DIOR <sub>i</sub> for uDMA data-in : MH_HDMARDY <sub>i</sub> for uDMA data-out : MH_HSTROBE
	MH_IORDY	O	80	Drive by X-Wall, one of the 3 signals is selected: for PIO : MH_IORDY for uDMA Data-In : MH_DSTROBE for uDMA Data-Out : MH_DDMARDY <sub>i</sub>
	MH_DIOW <sub>i</sub>	I	76	Driven by host, internally split into: for PIO : MH_DIOW <sub>i</sub> for uDMA, Data-In, Data-Out : MH_STOP
	MH_RESET <sub>i</sub>	I	125	Host reset signal
	MH_DASPI	O	127	Device active
	MH_PDIAG <sub>i</sub>	O	128	Passed diagnostics; cable assembly type identifier
	MH_CSEL	I	126	Cable select
<b>Device IDE Interface (To Hard Disk Drive)</b>	MD_CSi[1:0]	O	52,54	Chip select 0 & Chip select 1 driven by the X-Wall
	MD_DD[15:0]	IO	32-29,27,26,24,23,21,20,15,14,11,10,8,7	IDE Data Driven by both X-Wall and Device
	MD_DA[2:0]	O	42,45,47	IDE address driven by X-Wall
	MD_DMACK <sub>i</sub>	O	39	IDE DMA acknowledge driven by X-Wall
	MD_DMARQ	I	36	IDE DMA request driven by Device
	MD_INTRQ	I	34	IDE Interrupt request driven by Device
	MD_DIOR <sub>i</sub>	O	41	Drive by X-Wall, one of the 3 signals is selected: for PIO : MD_DIOR <sub>i</sub> for uDMA data-in : MD_HDMARDY <sub>i</sub> for uDMA data-out : MD_HSTROBE
	MD_IORDY	I	37	Drive by X-Wall, internal split into: for PIO : MD_IORDY for uDMA Data-In : MD_DSTROBE for uDMA Data-Out : MD_DDMARDY <sub>i</sub>
	MD_DIOW <sub>i</sub>	O	40	Driven by X-Wall, one of the 2 signals is selected: for PIO : MD_DIOW <sub>i</sub> for uDMA, Data-In, Data-Out : MD_STOP
	MD_RESET <sub>i</sub>	O	5	Driven by X-Wall, reset signal
	MD_DASPI	I	2	Device active
	MD_PDIAG <sub>i</sub>	I	1	Passed diagnostics; cable assembly type identifier
		MD_CSEL	O	3

<b>Power Pins</b>	VCC5		4,9,19,25,33,38,50,60,70,77,85,90,101,107,116,122	Power Supply (+5V)
	Vss		6,12,22,28,35,43,57,64,66,74,82,96,98,104,110,119	Ground
<b>Portable Key Interface</b>	SEEPROM_SK	O	83	Key serial data clock
	SEEPROM_CS	O	84	Key chip select
	SEEPROM_DI	O	86	Key serial data input
	SEEPROM_DO	I	87	Key serial data output
<b>Others</b>	CLK_Mode	I	61	Low: 33 MHz; High: 66 MHz
	CLOCK	I	62	33 MHz or 66 MHz
	DES_ENA	I	58	NC for encrypt/decrypt operation, low for by-pass mode
	KEY_ERR	O	49	Output high for key not existed or key parity error
	DEV_SEL	I	59	Device select; no connection for master, low for slave
	NC			13,16-18,44,46,48,51,53,55,56,63,68,69,78,81,89,91-95,112-114

### 3.3 Electrical Characteristics

- Operating Voltage (Vcc): +4.5V ~ +5.5V
- Temperature limit rating:
  - Storage temperature: -55°C ~ +125 °C
  - Operating temperature: 0°C ~ +70 °C
- PIO mode uses 40-conductor cable
- UDMA mode 0, 1, 2 uses 40-conductor cable
- UDMA mode 3,4,5 uses 80-conductor cable

## 4. Layout & Package Information

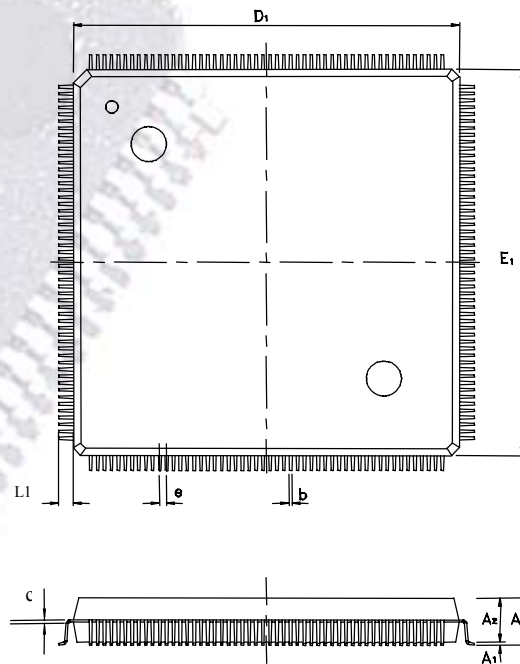
### 4.1 128-pin LQFP

LQFP (Low Profile Quad Flat Package) provides low profile with 1.4mm body thickness, suitable for space concerned applications. Package size 14×14mm and lead-count 128 are offered for portable, lightweight and low profile applications.

### 4.2 FEATURES

- ◆ 14×14mm body size with 128 lead count
- ◆ Copper leadframe
- ◆ Low profile 1.40mm body thickness
- ◆ JEDEC standard outlines

### 4.3 Outline & Dimension



Body Size	Lead Count	L/F Material	Lead Pitch	PKG Thk.	Stand Off	Body Thk.	Lead Length	Lead Width	L/F Thk.
D1 E1	N		e	A(Max.)	A1(Min.)	A2	L1	b	c
14 14	128	Cu:C7025	0.40	1.60	0.05	1.40	1.00	0.18	0.127

## 5. Platform Placement

Signal arrangement of the *X-Wall SE* is shown in Figure 7. Signal arrangement of *X-Wall SE*, whereas placement of the *X-Wall SE* is shown in Figure 8. Placement of add-on card.

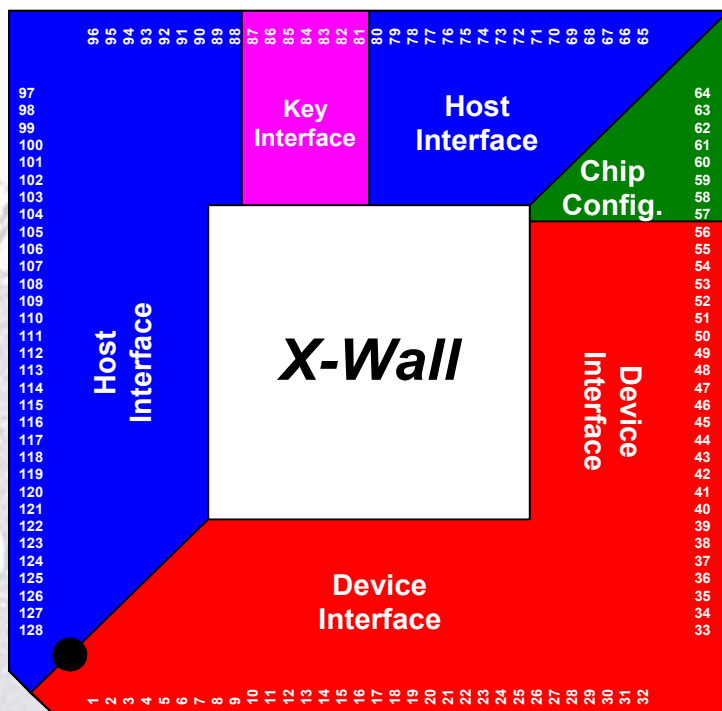


Figure 7. Signal arrangement of *X-Wall SE*

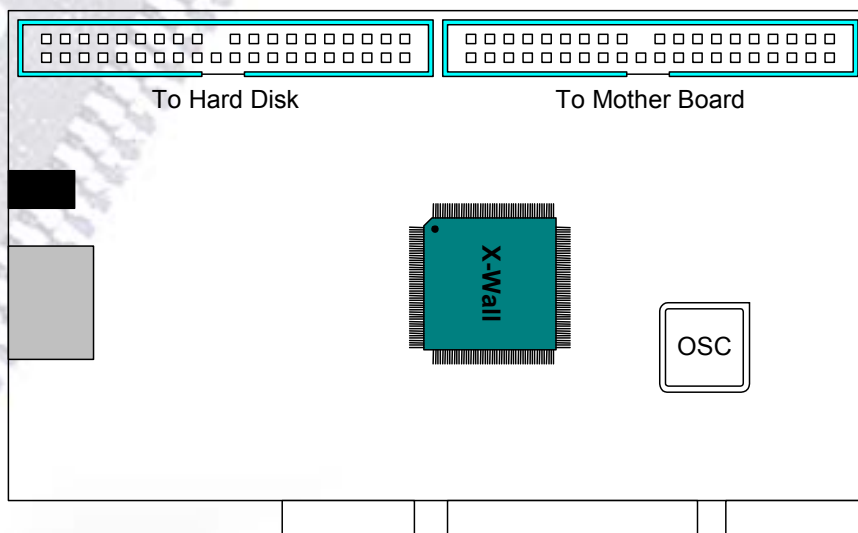


Figure 8. Placement of add-on card

## 6. Reliability Tests

### 6.1 Product Life Test

Test Items	Test Condition/Result	Reference Standard
Operating Life	TA=125°C ,1000Hours PASS	JESD22-A108-A

### 6.2 Electrical Test

Test Items	Test Condition/Result	Reference Standard
ESD	Level II	MIL-STD-883E 3015.7 JEDEC EIA/JESD22-A115
Latch-up	Level II	JEDEC-STD NO 78

### 6.3 Packaging Test

Test Items	Test Condition	Reference Standard
Thermal Shock	-65 Deg C/+150 Deg C 5min within 10 sec 5min 300 Cycles	MIL-STD-883E 1011.9
Temp. Cycling	-65 Deg C/+150 Deg C 1000 Cycles	MIL-STD-883E 1010.7
Pressure Cooker	121 Deg C,15 psig (2atm) 100% R.H. 216 hours	JEDEC-STD A102-2
Salt Atmosphere	35 Deg C,0.5%~3% NaCl PH6.5~7.2 24 hours	MIL-STD-883E 1009.8
HAST	TA=130 Deg C,85%R.H. 64 hours	JEDEC-STD NO. 22-A110

## 7. Marking Description

### **X-Wall SE-40NB**

SE NB – version  
40 – DES 40-bit strength

### **X-Wall SE-64NB**

SE NB – version  
64 – DES 64-bit strength

### **X-Wall SE-40A**

SE – version  
A -- upgrade  
128 – TDES 128-bit strength

### **X-Wall SE-64A**

SE – version  
A -- upgrade  
64 – DES 64-bit strength

### **X-Wall SE-128A**

SE – version  
A -- upgrade  
128 – TDES 128-bit strength

### **X-Wall SE-192A**

SE – version  
A -- upgrade  
192 – TDES 192-bit strength

### **0244-S**

0244 -- Year and Week of manufacturing date; Year 2002 on Week 44<sup>th</sup>  
S -- Package & assembly House; SPIL

**V60893.2** – Silicon Wafer Lot Number

## 8. Logistics

Package	Dimension	Capacity (Max.)
Tray	14*14*1.4 mm,6*15 grid, black	90ea
Inner Box	360*152*87 mm, white	900ea
Carton	375*333*290 mm, white	5400ea

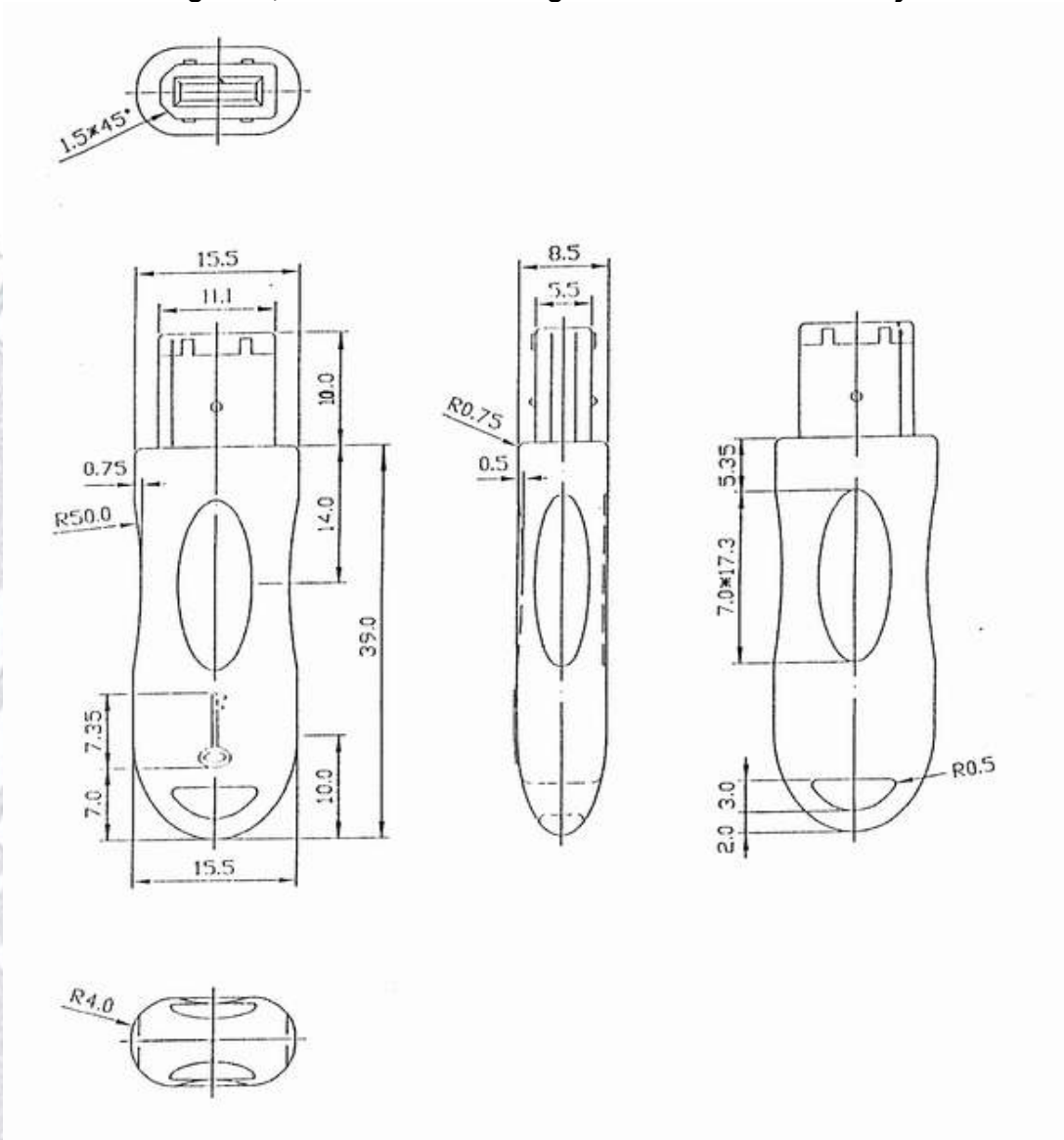
## 9. Standard Material

Chip	Non-epi wafer + TSMC process
Lead frame	Copper
Die Attach Adhesive	Silver paste
Bonding Wire	Gold
Encapsulant	Mold Compound
Lead Finish	85/15 Sn/Pb

## 10. Secure Key Specification

The X-Wall Secure Key as shown in Figure 9, the Mechanical Drawing of Secure Key, has been used as an authentication utility to store the required Secret Key of the X-Wall DES/TDES encryption engine. The X-Wall will not be functional without the proper insertion of the X-Wall Secure Key at the stage of system boot up. The Secret Key length varies, ranging from 40-bit all the way up to 192-bit. The bit length stored inside the Secure Key depends on various X-Wall chips chosen.

Figure 9, Mechanical Drawing of the X-Wall Secure Key



<b>Specification</b>	<b>6 Pin 1394 type connector</b>
<b>Dimension</b>	<b>As attached</b>
<b>Materials</b>	<b>Inner Molding: PE Package Molding: PVC</b>
<b>Colors</b>	<b>Blue or Purple</b>
<b>Operating Temperature</b>	<b>-20 degree C to +80 degree C</b>
<b>Operating Voltage</b>	<b>DC +3.3 to 5V</b>
<b>Power Consumption</b>	<b>&lt; 0.03W</b>
<b>Weight per key</b>	<b>8.5g</b>