

## Table of Selection of X-Wall Hardware Real-time Cryptographic Processor

| Available Product SKU   | X-Wall CO-128<br>X-Wall CO-192  | X-Wall MX-128<br>X-Wall MX-192<br>X-Wall MX-256<br>X-Wall MX-128C<br>X-Wall MX-192C<br>X-Wall MX-256C    | X-Wall FX-128<br>X-Wall FX-192<br>X-Wall FX-256<br>X-Wall FX-128C<br>X-Wall FX-192C<br>X-Wall FX-256C    | X-Wall DX-128<br>X-Wall DX-128C<br>X-Wall DX-256<br>X-Wall DX-256C                                      |
|---|---|--|--|---|
| <b>Categories</b>   |   |  |  |   |
| <b>Year Introduced</b>  | 2006/7  | 2007/8   | 2008/9   | 2010/11   |
| <b>Built-in Interface Controller</b>  | ATA/ATA   | SATA/SATA  | USB2.0/SATA  | USB2.0/USB2.0   |
| Production Units Availability   | Yes   | Yes  | Yes  | Yes   |
| <b>Product Warranty 3 Years</b>   | Yes   |  | Yes  |   |
| <b>Product Warranty 5 years</b>   |   | Yes  |  | Yes   |
| <b>Operating Temperature</b>  | -40C to +90C  | -45 to +90C  | Standard   | Standard  |
| High Temperature Operating Life (HTOL)  | 1,000 hours @125C   | 1,000 hours @125C  | Yes  | Yes   |
| <b>NIST &amp; CSE certified Cryptographic Engine</b>  | TDES<br>128/192-bit   | AES ECB/CBC up to 256-bit  | AES ECB/CBC 256-bit  | AES ECB/CBC up to 256-bit   |
| <b>FIPS 140-2 Certified</b>   |   | Yes  |  | In Progressing  |
| Design Guide version  | Version 1.0   | Version 2.2  | Version 1.0  | Version 1.2   |
| Reference Schematics & Layout (OrCAD)   | Yes   | Yes  | Yes  | Yes   |
| Development Board Availability  | Yes, on order   | Yes, on order  | Yes, on order  | Yes, on order   |
| Authentication is a matter of deciding when the secret key is released by:<br><ul style="list-style-type: none"> <li>• Smartcard, Fingerprint, Password, or Key Token</li> </ul> All the designers need to do is to decide when to release the secret key to enable the X-Wall crypto engine. | Single or Multi-Factor Authentication, which is design dependent.                           | <b>Pre-boot password authentication software as part of a BIOS or OS kernel code is available.</b>       | Single or Multi-Factor Authentication, which is design dependent.  | Single or Multi-Factor Authentication, which is design dependent.                                       |
| Interface for secret key loading  | <ul style="list-style-type: none"> <li>• 2-wire SEEPROM;</li> <li>• Built-in API</li> </ul> | <ul style="list-style-type: none"> <li>• Built-in API;</li> <li>• Source codes for developers</li> </ul> | <ul style="list-style-type: none"> <li>• Built-in API;</li> <li>• Source codes for developers</li> </ul> | <ul style="list-style-type: none"> <li>• Built-in API</li> <li>• USB Vendor Specific Command</li> </ul> |
| <b>Upgradeable Firmware</b>   |   |  |  | YES   |
| <b>Volatile Type Key Registers</b>  | Yes. Loss secret key at power off.  | Yes. Loss secret key at power off.   | Yes. Loss secret key at power off.   | Yes. Loss secret key at power off.  |
| API software availability   | Yes, Linux & x86  | Yes, Linux & x86   |  | Windows & MAC   |
| <b>Burst (Max.) Current Consumption</b>   |   | ~ 219mA @1.8V  | ~ 212mA @1.8V  | ~ 100mA @1.8V   |
| <b>IC Package</b>   | 128-pin LQFP  | 80-pin TQFP  | 64-pin TQFP  | 48-pin TQFP   |
| Core Voltage  | 3.3V  | 1.8V   | 1.8V   | 1.8V  |
| Hard Drive & SSD support  | > 137GB   | SATA > 2TB   | Over 2TB   | Over 2TB  |
| Sustained Real-time Crypto Engine Throughput  | > 1.2 Mbit/sec  | > 120MB/sec  | > 30MB/sec   | > 30MB/sec  |
| RoHS & Lead-free compliance   | Yes   | Yes  | Yes  | Yes   |
| Pin Compatibility?  | All CO & XO chips share the same pin definition   | All MX series share the same pin definition  | All FX series share the same pin definition.   | All DX series share the same pin definition.  |